Claims

[c1] 1. A method, comprising:
identifying at least one electrical characteristic for an alpha device;
identifying the at least one electrical characteristic for a plurality of dependent devices;
and
identifying a group comprising the alpha device and the plurality dependent devices
comprising the at least one electrical characteristic for associated manufacturing testing.

[c2] 2. The method of claim 1, further comprising grouping the alpha device and the plurality of dependent devices together on a semiconductor device for the associated manufacturing testing.

[c3] 3. The method of claim 2, wherein said grouping comprises electrically connecting the alpha device to the plurality dependent devices during the associated manufacturing testing.

[c4] 4. The method of claim 3, further comprising electrically disconnecting the alpha device from the plurality depen-

dent devices upon completion of the associated manufacturing testing.

[c5] 5. The method of claim 2, further comprising providing by the alpha device, a first signal adapted to operate the plurality of dependent devices during the associated manufacturing testing.

[c6] 6. The method of claim 5, further comprising providing a second signal adapted to operate the plurality of dependent devices during the associated manufacturing testing; and
multiplexing between the first signal and the second signal during the associated manufacturing testing.

[c7] 7. The method of claim 2, further comprising testing the plurality of dependent devices simultaneously in parallel during the associated manufacturing testing.

[c8] 8. The method of claim 2, further comprising testing the plurality of dependent devices individually during the associated manufacturing testing.

[c9] 9. The method of claim 2, wherein the alpha device and the plurality of dependent devices are cores on the semiconductor device.

[c10] 10. The method of claim 2, wherein the semiconductor

device is an application specific integrated circuit (ASIC).

[c11] 11. The method of claim 1, wherein the at least one electrical characteristic comprises an operational frequency of the plurality of dependent devices.

[c12] 12. The method of claim 11, wherein the operational frequency comprises a range of about 1 gigahertz to about 6 gigahertz.

[c13] 13. The method of claim 1, wherein the at least one electrical characteristic comprises a jitter tolerance of the plurality of dependent devices.

[c14] 14. The method of claim 1, wherein the alpha device comprises a phase lock loop circuit.

[c15] 15. The method of claim 14, wherein each of the plurality of dependent devices comprise a serializer/deserializer (SerDes) circuit.

[c16] 16. The method of claim 1, wherein the associated manufacturing testing comprises testing the plurality of dependent device for functional operation.

[c17] 17. The method of claim 16, wherein the associated manufacturing testing comprises testing the plurality of dependent devices for the functional operation within a design specification.

[c18] 18. The method of claim 17, wherein the design specification is a frequency range.

[c19] 19. The method of claim 17, wherein the design specification is a speed at which the plurality of dependent devices perform the functional operation.

[c20] 20. The method of claim 1, wherein the plurality of dependent devices is selected from the group consisting of an analog to digital convertor, a digital to analog convertor, and a BIST engine.